Amendments to the Specification

Kindly amend the paragraph appearing a page 11, lines 1-11, as follows:

In the field effect transistor manufacturing method in the first embodiment which utilizes a SIMOX wafer achieved by forming a buried oxide film (BOX) 2 and a silicon layer 3 over thicknesses of approximately 110mm and 50nm respectively on a silicon substrate 1, an oxide film 4 is formed over a thickness of 7nm through oxidation on the silicon layer 3, a silicon nitride film (SiN) ~~5a~~ is formed over a thickness of 160nm through a CVD method on the oxide film 4, a resist pattern (not shown) to be utilized as a mask when patterning an element isolation area is formed, any unnecessary areas of the SiN film ~~5a~~ and the oxide film 4 are etched by using the resist pattern as a mask and, as a result, an active nitride film 5 is formed (FIG. 1(A)).

Kindly amend the paragraph appearing a page 14, lines 1-16, as follows:

In the field effect transistor manufacturing method in the second embodiment which utilizes a SIMOX wafer achieved by forming a buried oxide film 2 and a silicon layer 3 over thicknesses of approximately 110nm and 50nm respectively on a silicon substrate 1, an oxide film 4 is formed over a thickness of 7nm through oxidation on the silicon layer 3, a silicon nitride film ~~5a~~ is formed over a thickness of 120nm through a CVD method on the oxide film 4, a resist pattern (not shown) to be utilized as a mask when patterning an element isolation area 6 is formed, any unnecessary areas of the silicon nitride film ~~5a~~ and the oxide film 4 are etched by using the resist pattern as a mask and, as a result, an active nitride film 5 is formed. The second embodiment differs from the first embodiment in the film thickness of the silicon nitride film ~~5a~~ which is reduced in the second embodiment. While the silicon layer 3 also becomes etched as the

silicon nitride film ~~5a~~ is etched, the extent to which the silicon layer 3 is ground can be lessened by reducing the SiN film thickness (FIG. 1(A)).

Kindly amend the paragraph bridging pages 14 and 15 as follows:

Then, a wet-etching process is implemented by using hydrofluoric acid (HF) in order to remove the oxide film formed at the surface of the silicon nitride film ~~5a~~, and the active nitride film 5 is wet-etched over approximately 60nm with hot phosphoric acid. Since isotropic etching is implemented during the wet-etching process, the film thickness becomes reduced by 60nm to approximately 60nm and the edge 7 of the active nitride film 5 recede by approximately 60nm as well. Through this etching process, the edge 7 of the silicon layer 3 becomes partially exposed from under the active nitride film 5' (FIG. 1(C)).

Kindly amend the paragraph appearing a page 16, lines 14-24, as follows:

In the field effect transistor manufacturing method in the third embodiment which utilizes a SIMOX wafer achieved by forming a buried oxide film 2 and a silicon layer 3 over thicknesses of approximately 110mm and 50nm respectively on a silicon substrate 1, an oxide film 4 is formed over a thickness of 7nm through oxidation on the silicon layer 3, a silicon nitride film ~~5a~~ is formed over a thickness of 100nm through a CVD method on the oxide film 4, a resist pattern (not shown) to be utilized as a mask when patterning an element isolation area 6 is formed, any unnecessary areas of the silicon nitride film ~~5a~~ and the oxide film 4 are etched by using the resist pattern as a mask and, as a result, an active nitride film 5 is formed (FIG. 4(A)).

Kindly amend the paragraph appearing a page 20, lines 8-18, as follows:

In the field effect transistor manufacturing method in the fifth embodiment which utilizes a SIMOX wafer achieved by forming a buried oxide film 2 and a silicon layer 3 over thicknesses of approximately 110mm and 50nm respectively on a silicon substrate 1, an oxide film 4 is formed over a thickness of 7nm through oxidation on the silicon layer 3, a silicon nitride film ~~5a~~ is formed over a thickness of 160nm through a CVD method on the oxide film 4, a resist pattern (not shown) to be utilized as a mask when patterning an element isolation area 6 is formed, any unnecessary areas of the silicon nitride film ~~5a~~ and the oxide film 4 are etched by using the resist pattern as a mask and, as a result, an active nitride film 5 is formed (FIG. 6(A)).

Kindly amend the paragraph bridging pages 23 and 24 as follows:

In the field effect transistor manufacturing method in the sixth embodiment which utilizes a SIMOX wafer achieved by forming a buried oxide film 2 and a silicon layer 3 over thicknesses of approximately 110mm and 50nm respectively on a silicon substrate 1, an oxide film 4 is formed over a thickness of 7nm through oxidation on the silicon layer 3, a silicon nitride film ~~5a~~ is formed over a thickness of 160nm through a CVD method on the oxide film 4, a resist pattern (not shown) to be utilized as a mask when patterning an element isolation area is formed, any unnecessary areas of the silicon nitride film ~~5a~~ and the oxide film 4 are etched by using the resist pattern as a mask and, as a result, an active nitride film 5 is formed (FIG. 8(A)).

Amendments to the Drawings

Attached are four (4) replacement sheets of drawings for FIGS. 17-20. Each of these figures has been amended to include the label "PRIOR ART."